REMARKS

The Office Action dated September 10, 2004, has been received and reviewed.

Claims 1-12 and 14 are currently pending and under consideration in the above-referenced application. Each of claims 1-12 and 14 stands rejected.

Reconsideration of the above-referenced application is respectfully requested.

Preliminary Amendment

Please note that a Preliminary Amendment was filed in the above-referenced application on March 4, 2004, but that the undersigned attorney has not yet received any acknowledgement that the Preliminary Amendment has been entered into the Office file for the above-referenced application. If, for some reason, the Preliminary Amendment has not yet been entered into the Office file, the undersigned attorney would be happy to provide the Office with a true copy thereof.

Objection to the Title

The title of the above-referenced application was objected to for not accurately reflecting the subject matter to which the claims are directed.

The title has been revised to reflect the subject matter recited in the claims. Accordingly, withdrawal of the objection to the title is respectfully requested.

Objections to the Specification

The specification was objected to because the term "features" is purportedly unclear. The "features" to which the Office is apparently referring are "features 29" of a mask 28, which is discussed, among other places, at paragraph **[0040]** of the specification.

Paragraph **[0040]** has been amended to provide an example of the "features 29" mentioned therein. Specifically, paragraph **[0040]** has been amended to indicate that walls that define apertures of the mask 28 are an example of the "features 29" referred to in that paragraph.

It is respectfully submitted that the revision to paragraph [0040] does not introduce new matter into the above-referenced application, as one of ordinary skill in the art would readily

appreciate that the only features of masks used in semiconductor device fabrication processes are the solid portions of such masks and the walls of such solid portions that define the apertures through such masks. *See, e.g.,* Peter Van Zant, "Microchip Fabrication," pages 162-167 and 237-239 (2d Ed., 1990).

The specification has also been objected to because it allegedly does not provide support for the recitation of "at most about 1¼ in-film particles or surface roughness features per square millimeter of surface area" in independent claims 1 and 8.

It is respectfully submitted that the specification does provide support for this subject matter. Specifically, the specification, at paragraph **[0019]**, for example, discloses semiconductor device structures that have "an imperfection density of less than about 40,000 particles of about 120-150 nm dimension per eight inch diameter semiconductor wafer . . ." It is evident from paragraph **[0019]** and elsewhere in the specification of the above-referenced application that "imperfections" include "in-film particles and non-uniformities." Simple geometry and mathematics may be used to determine the maximum number of such imperfections per area. Since the diameter (d) and, thus, the radius (r) ($r = d/2$) of an eight inch diameter semiconductor wafer are known, the area (a) of such a wafer may be readily determined (*i.e.,* $a = \pi r^2$). Eight inches is equivalent to about 200 mm. Thus, an eight inch diameter wafer may also be referred to as a 200 mm diameter wafer. The radius of such a wafer is 4 inches, or about 100 mm. The area, in square millimeters (mm^2), of such a wafer is about 31,400 mm^2 (more precisely, 32,429 mm^2). The maximum imperfection density per square millimeter may then be determined by dividing the total maximum imperfection density per eight inch wafer by its area, in square millimeters (*i.e.,* 40,000 particles or surface roughness features / 31,400 mm^2). The result is a maximum imperfection density of 1.27, or about 1¼, particles or surface roughness features per square millimeter.

Therefore, the specification of the above-referenced application clearly provides support for the recitation of "at most about 1¼ in-film particles or surface roughness features per square millimeter of surface area" in independent claims 1 and 8.

The specification has also been objected to for assertedly failing to provide support for the recitation of "times the sum of x, y, and z" in claims 4 and 11.

Exemplary support for this recitation is provided in paragraph **[0034]** of the specification. In particular, paragraph **[0034]** states than x + y + z may equal 1, and provides exemplary ranges and values for each of x, y, and z. Thus, it is apparent from such disclosure that the relative values of x, y, and z and, thus, the relative amounts of Si, O, and N may be determined by multiplying the value ranges provided in claims 4 and 11 by the sum of x, y, and z (*e.g.*, one).

As such, it is respectfully submitted that the specification of the above-referenced application supports the subject matter recited in claims 4 and 11.

In view of the foregoing, withdrawal of the objection to the specification is respectfully requested.

Claim Objection

The Office has objected to independent claim 8 for reciting "nonometers." This was merely a typographical error which has been corrected by revising independent claim 8 to recit "nanometers." Additionally, another typographical error in independent claim 8 has been corrected by replacing the term "of" on line 4 with "or."

It is respectfully requested that the objection to independent claim 8 be withdrawn.

Rejections Under 35 U.S.C. § 112, Second Paragraph

Claims 1-12 and 14 have been rejected under 35 U.S.C. § 112, second paragraph, for allegedly being indefinite.

It has been asserted that several elements of claims 1-12 and 14 are indefinite.

In particular, it has been asserted that the recitation of "at most about 1¼ in-film particles" in independent claims 1 and 8 is indefinite. When read in context, it is clear that independent claims 1 and 8 recite that there may be, on average, a maximum of about 1¼ in-film particles or surface roughness features per square millimeter of surface area of the srecited semiconductor device structure. Thus, the recitation "at most about 1¼ in-film particles" in

independent claims 1 and 8 complies with the definiteness requirement of 35 U.S.C. § 112, second paragraph.

It has also been alleged that the recitation "roughness features . . . per square millimeter of surface area" is indefinite. Again, when considered in context, it is clear that independent claims 1 and 8 are merely defining a maximum average number (1¼ per square millimeter) of in-film particles or surface roughness features that may be present on the surface of a semiconductor device structure. Therefore, one of ordinary skill in the art would consider the recitation "roughness features . . . per square millimeter of surface area" to be definite.

The Office also asserts that the recitation "in-film particles or surface roughness features of at least 120 nanometers size . . ." in independent claim 8 is indefinite. It is not understood how such an asserted could be made. The dimension set forth in independent claim 8 (*i.e.*, "at least 120 nanometers") is abundantly clear. This number refers to a dimension, or the size across, an in-film particle or surface roughness feature. The specification of the above-referenced application includes a lengthy discussion of various examples of the types and sizes of imperfections, including in-film particles (*e.g.*, contaminants – *see, e.g.*, paragraph **[0014]**; imperfections in a fabricated layer—*see, e.g.*, paragraph **[0036]**; etc.) and surface roughness features (*e.g.*, non-uniformities on the surface of a material layer – *see, e.g.*, paragraph **[0019]**) having a dimension of about 120-150 nm, that are reduced in number and density when the processes that are disclosed in the above-referenced application are effected. Accordingly, the recitation of independent claim 8 "in-film particles or surface roughness features of at least 120 nanometers size . . ." complies with the definiteness requirement of 35 U.S.C. § 112, second paragraph.

The phrase "measurable particulates" in claims 5 and 12 is also purportedly indefinite. One of ordinary skill in the art would readily understand the characteristics (*e.g.*, size, composition, etc.) of particulates that would render them measurable or immeasurable. For example, "measurable particulates" may have dimensions of less than about 120 nm (*see, e.g.*, paragraph **[0018]**), or dimensions of about 120 nm to about 150 nm (*see, e.g.*, paragraph **[0019]**). Therefore, claims 5 and 12 are sufficiently definite to meet the requirements of 35 U.S.C. § 112, second paragraph.

It has also been asserted that the phrase "times the sum of x, y, and z . . ." in claims 4 and 11 is indefinite. Paragraph **[0034]** of the specification uses these values in an exemplary manner to indicate the relative percentages of Si, O, and N that are present in a material, where $x + y + z = 1$. Of course, one of ordinary skill in the art would readily understand that x, y, and z, which respectively denote the relative numbers of Si, O, and N atoms present in a molecule or material, may in reality only be whole numbers. It is inherent that the fractions of Si, O, and N atoms present in a material is equal to the respective numbers (*i.e.,* x, y, and z) of each of Si, O, and N atoms present in the material, divided by the total number of atoms present in the material (*i.e.,* x+y+z). Inversely, the number (*i.e.,* x, y, and z) of atoms of each of Si, O, and N in a particular material may inherently be determined by multiplying the fraction or percentage that corresponds to that type of atom by the total number of atoms present in the material (*i.e.,* x+y+z).

For example, from the description provided in paragraph **[0034]**, one of ordinary skill in the art would readily recognize the variations of $Si_xO_yN_z$ that would fall within the scope of claims 4 and 11. Examples of materials that fall within the scope of claims 4 and 11 include Si_2ON (where x+y+z=4, x (2) = 0.5 × 5, y (1) = 0.25 × 4, and z (1) = 0.25 × 4), Si_3ON (where x+y+z=5, x (3) = 0.6 × 5, y (1) = 0.2 × 5, and z (1) = 0.2 × 5), and Si_3O_2N (where x+y+z=6, x (3) = 0.5 × 6, y (2) = 0.333 × 6, and z (1) = 0.167 × 6).

As claims 4 and 11 recite this inherent concept very clearly, there does not appear to be any basis for the Office's assertion that this recitation in claims 5 and 12 is indefinite. Therefore, claims 4 and 11 comply with the definiteness requirement of 35 U.S.C. § 112, second paragraph.

Claims 2, 3, 6, 7, 9, 10, and 14 have been rejected merely for depending from rejected claims.

In view of the foregoing, it is respectfully requested that the 35 U.S.C. § 112, second paragraph, rejections of claims 1-12 and 14 be withdrawn.

Moreover, the specification of the above-referenced application provides some guidance as to the meanings of the phrases "in-film particles" and "surface roughness features."

Rejections Under 35 U.S.C. § 103(a)

Claims 1-12 and 14 stand rejected under 35 U.S.C. § 103(a) for reciting subject matter which is assertedly unpatentable over the Prior Art depicted in Fig. 4 of the above-referenced application (hereinafter "the PA").

The standard for establishing and maintaining a rejection under 35 U.S.C. § 103(a) is set forth in M.P.E.P. § 706.02(j), which provides:

> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

It has been asserted that, while the PA does not teach or suggest "at most about 1¼ in-film particles or surface roughness features . . . per square millimeter of surface area," "[t]he law is replete with cases in which the difference between the claimed invention and the prior art is some range or other variable within the claims" Office Action, page 4, citing *In re Woodruff*, 919 F.2d 1575, 16 USPQ2d 1934 (Fed. Cir. 1990). It has been further asserted that "In such a situation, the applicant must show that the particular range is critical, generally by showing that the claimed range achieves unexpected results relative to the prior art range." *Id.*

This law has not been properly applied. M.P.E.P. § 2144.05, where *Woodruff* is cited, and *Woodruff* itself are limited to cases where a range recited in a claim overlaps a range in the prior art. The Office has not submitted any prior art that teaches or suggests a range that overlaps the ranges recited in independent claims 1 and 8 of the above-referenced application. Nor has the Office provided any other prior art teaching or suggestion that would tend to show that a semiconductor device structure including a layer comprising silicon nitride and "at most about 1¼ in-film particles or surface roughness features . . . per square millimeter of surface

area" would have been obvious to one of ordinary skill before the priority date for the above-referenced application.

Therefore, the Office has not established a *prima facie* case of obviousness against either independent claim 1 or independent claim 8. As such, under 35 U.S.C. § 103(a), independent claims 1 and 8 are both allowable over the PA.

Claims 2-7 are each allowable, among other reasons, for depending directly or indirectly from claim 1, which is allowable.

Each of claims 9-12 and 14 is allowable, among other reasons, for depending directly or indirectly from claim 8, which is allowable.

Claims 5 and 12 are additionally allowable because the PA does not teach or suggest a semiconductor device structure that includes a first layer that "is substantially free of at least one of measurable particulates and surface roughness."

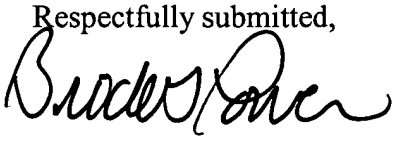
Claim 6 is further allowable because the PA lacks any teaching or suggestion of a semiconductor device structure that includes a layer comprising silicon nitride that includes "at most about 1¼ of at least one o particles and surface roughness features of at least about 120 nm dimension per square millimeter of surface area."

For these reasons, it is respectfully requested that the 35 U.S.C. § 103(a) rejections of claims 1-12 and 14 be withdrawn, and that each of these claims be allowed.

CONCLUSION

It is respectfully submitted that each of claims 1-12 and 14 is allowable. An early notice of the allowability of each of these claims is respectfully solicited, as is an indication that the above-referenced application has been passed for issuance. If any issues preventing allowance of the above-referenced application remain which might be resolved by way of a telephone conference, the Office is kindly invited to contact the undersigned attorney.

Respectfully submitted,



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Chapter

8

Photolithography—Preparation to Exposure

Overview

In this chapter the all-important photolithography processes are detailed. The chapter starts with an explanation of a basic ten-step process and includes a discussion on photoresist chemistry and physical parameters. The majority of the chapter is devoted to the process steps from surface preparation to alignment and exposure. Each of the options available for the steps is explained and evaluated.

Objectives

Upon completion of this chapter, you should be able to:

1. Sketch wafer cross sections showing the basic ten-step photomasking process.
2. Explain the reaction of negative and positive photoresists to light.
3. Describe the correct resist and mask polarities required to produce holes and islands in wafer surface layers.
4. Make a list of the major process options for each of the ten basic steps.
5. Select from the list in objective 4 the processes used to pattern features in micron and submicron sizes.
6. Describe the need for, and process steps used in, double masking, multilayer resist processing, and planarization techniques.

7. Explain the use of antireflective coatings and contrast enhancement in the patterning of "small" feature sizes.
8. List the optical and nonoptical methods used for alignment and exposure.
9. Compare the equipment and advantages of each alignment and exposure method.

Introduction

Photolithography is one of the terms used to identify the basic operation of patterning. Other terms used are *photomasking, masking, oxide* or *metal removal* (OR, MR), and *microlithography*. (Recall that patterning is the process that removes specific portions of the top layer(s) on the wafer surface. See Fig. 8.1.).

Photolithography is one of the most critical operations in semiconductor processing. It is the patterning process that sets the horizontal dimensions on the various parts of the devices and circuits. The goal of the operation is twofold. First, is to create in and on the wafer surface a pattern whose dimensions are as close to the design requirements as possible. This goal is referred to as the *resolution* of the images on the wafer. The pattern dimensions are referred to as the *feature sizes* or *image sizes* of the circuit.

The second goal is the correct placement (called *alignment* or *registration*) of the circuit pattern on the wafer. The entire circuit pattern

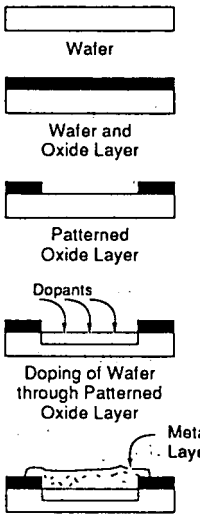

Figure 8.1 Basics of silicon planar processing.

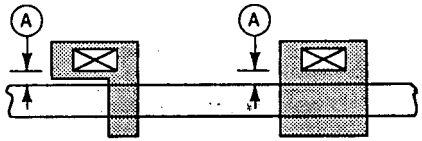

Figure 8.2 Minimum spacings (registration) for contact and metal patterns.

must be correctly placed on the wafer surface and the individual parts of the circuit must be in the correct positions relative to each other. Keep in mind that the final pattern is created from several photomasks applied to the wafer in a sequential manner. The registration requirement is similar to the correct stacking of the different floors of a building in relation to each other. It is easy to imagine the effect on the functioning of a stairwell or elevator if the floors of a building did not sit directly on top of each other. In a circuit, the effects of a misaligned mask layer can cause the entire circuit to fail.

For VLSI and ULSI work, the resolution and registration requirements are very stringent. A VLSI circuit with micron or submicron feature sizes must be formed on the wafer surface with tolerances of ± ⅓ μm. The patterns must register to each other to a specification of 0.1 μm^1 as illustrated in Fig. 8.2.

Overview of the Photomasking Process

Photolithography is a multistep pattern transfer process similar to stenciling or photography. In photolithography the required pattern is first formed in reticles or photomasks and transferred into the surface layer(s) of the wafer through the photomasking steps.

The transfer takes place in two steps. First, the pattern on the reticle or mask is transferred into a layer of photoresist (Fig. 8.3). Photoresist is a light-sensitive material similar to the coating on a regular photographic film. It changes its structure and properties when exposed to light. In the example in Fig. 8.3, the photoresist in the region exposed to the light was changed from a soluble condition to an insoluble one. Resists of this type are called *negatively acting* and the condition change is called *polymerization*. Removing the soluble portion with chemical solvents (developers) leaves a hole in the resist layer that corresponds to the opaque pattern on the reticle.

The second transfer takes place from the photoresist layer into the wafer surface layer (Fig. 8.4). The transfer occurs when the wafer etchants remove the portion of the wafer's top layer that is not covered with photoresist. The chemistry of photoresists is such that they do not dissolve in the chemical etching solutions; they are *etch-resistant*.

Process Step	Purpose	Cross Section
Alignment and Exposure	Precise alignment of mask to wafer and exposure to u.v. light. Negative resist is polymerized.	
Development	Removal of unpolymerized resist.	

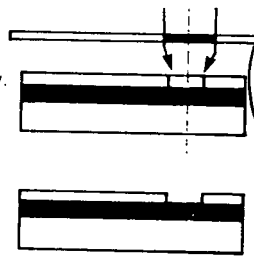

Figure 8.3 First pattern transfer—from mask to resist layer.

Process Step	Purpose	Cross Section
Etch	Selective removal of top surface layer	
Photoresist Removal	Clean photoresist from the wafer surface	
Final Inspection	Inspection of wafer for correctness of image transfer from photoresist to top layer	

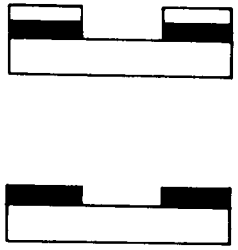

Figure 8.4 Second image transfer.

In the example shown in Figs. 8.3 and 8.4, the result is a hole etched in the wafer layer. The hole came about because the pattern in the mask was opaque to the exposing light. A mask whose pattern exists in the opaque regions is called a *clear-field mask* (Fig. 8.5). The pattern could also be coded in the mask in the reverse, in a dark-field mask. If the same steps were followed, the result of the process would be an island of material left on the wafer surface (Fig. 8.6).

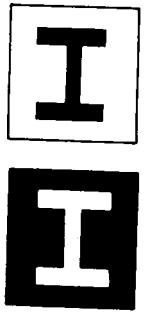

Figure 8.5 Mask-reticle polarities.

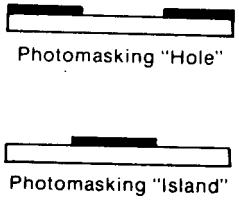

Figure 8.6 Photomasking hole and island.

Process Step	Purpose	Cross Section
Alignment and Exposure	Precise alignment of mask to wafer and exposure to u.v. light. Negative resist is polymerized.	
Development	Removal of unpolymerized resist.	

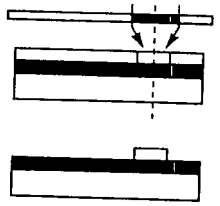

Figure 8.7 First image transfer from a light-field mask to a positive photoresist layer.

The resist reaction to light just described is a character of negative-acting photoresists. There are also positive-acting photoresists. Within these resists, the light changes the chemical structure from relatively nonsoluble to much more soluble. The term describing this change is *photosolubilization*. Figure 8.7 shows that an island is produced when a light-field mask is used with a positive photoresist.

The result obtained from the photomasking process from different combinations of mask and resist polarities is shown in Fig. 8.8. The choice of mask and resist polarity is a function of the level of dimensional control and defect protection required to make the circuit work. These issues are discussed in the process sections of the chapter.

Ten-Step Process

Transferring the image on the reticle or mask into the wafer surface layer requires a number of steps (Fig. 8.9). There are ten basic steps with many variations. The process illustrated is shown with a light-field mask and a negative photoresist. It is broken into two sections. The first section, steps 1 to 7, shows the first transfer. Steps 8, 9, and 10 finish the image transfer into the wafer surface layer.

Understanding this basic process is facilitated by making a list of the steps and drawing in the corresponding cross section. It is also instructive to draw cross sections but to change the polarity of the mask

		Photoresist Polarity	
		Negative	Positive
MASK POLARITY	Clear Field	HOLE	ISLAND
	Dark Field	ISLAND	HOLE

Figure 8.8 Mask and photoresist polarity results.

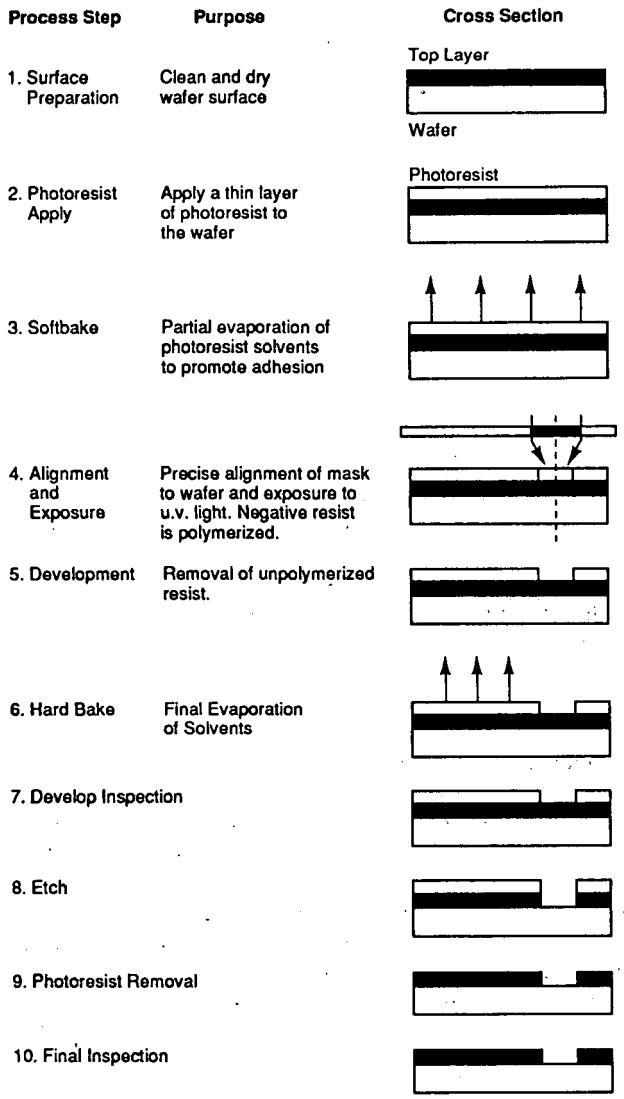

Figure 8.9 Ten-step photomasking process.

and photoresist. Mastering the steps and results using different resist and mask polarities will facilitate understanding the more in-depth explanations in the individual process sections.

Photoresist Chemistry

Photoresists have been used in the printing industry for over a century. In the 1920s photoresists found wide application in the printed circuit board industry. The semiconductor industry adapted this technology to wafer fabrication in the 1950s. Development of photoresists specifically designed for semiconductor use was first supplied by the Eastman Kodak Company. In the late 1950s, they introduced their line of KPR and KMER negative resists. At around the same time, the Shipley Company introduced a line of positive-acting resists. Since then a host of other companies have entered the market with photoresists designed to keep pace with ever-increasing industry demands to print narrower lines with fewer defects and at higher production rates. Today, the photoresist practitioner has available a wide range of products designed to match a variety of needs.

The photoresist is the heart of the masking process. The various steps are fine-tuned to accommodate the particular resist used and the desired results. The selection of a resist and development of a resist process is a detailed and lengthy procedure. Once a resist process is established, it is changed very reluctantly. Rarely will a photoresist engineer risk losing an entire process if only a marginal gain is possible with a new photoresist.

Photoresist composition

Photoresists are manufactured for both general and specific applications. They are tuned to respond to specific wavelengths of light and different exposing sources. They are given specific thermal flow characteristics and formulated to adhere to specific surfaces. These properties come about from the type, quantity, and mixing procedures of the chemical components in the resist. However, all the resists contain four basic ingredients (Fig. 8.10).

Light-sensitive and energy-sensitive polymers. The ingredients that contribute the photosensitive properties to the photoresist are special polymers. Polymers are groups of large, heavy molecules containing carbon, hydrogen, and oxygen that are formed into a repeated pattern. Plastics are a form of polymers.

The techniques of polymer chemistry impart the properties of specific light and radiation sensitivity into the polymer. The most commonly used resists react to some form of light energy: ultraviolet or

layer that has not been hard-baked is easily removed from the wafer with a simple acetone soak. In fact, acetone has been the traditional positive resist stripper. Unfortunately, acetone represents a fire hazard and its use is discouraged.

Several chemical manufacturers supply positive-only strippers based on the solvent *N*-methyl pyrrolidine (NMP).[10] These strippers are effective, water-rinsable, and drain-dumpable. For processes that include a positive resist hard bake, some of the solvent strippers can be heated to increase the removal rate. Figure 9.27 is a table of the most common wet resist strippers and their uses.

Dry stripping

Like etching, the dry plasma process can also be applied to resist stripping. The wafers are placed in a barrel chamber and oxygen is introduced (Fig. 9.28). The plasma field energizes the oxygen to a high-energy state, which, in turn, oxidizes the resist components to gases that are removed from the chamber by the vacuum pump.

$$C_xH_y \text{ (resist)} + O_2 \text{ (plasma energized)} \rightarrow CO \text{ (gas)} + CO_2 \text{ (gas)} + H_2O$$

Figure 9.28 Resist removal by plasma oxygen.

The major advantage of plasma resist stripping is the elimination of wet hoods and the handling of chemicals. The principal disadvantage is its ineffectiveness in the removal of metallic ions. There is not enough energy in the plasma field to volatilize the metallic ions. Another consideration of plasma stripping is radiation damage to the circuits from the high-energy plasma field. This problem is reduced with system designs that have the plasma chamber removed from the stripper chamber. They are called *downstream strippers* because the plasma is created downstream from the wafers. MOS wafers are more sensitive to radiation effects during stripping. Some companies use a dry plasma strip followed by a wet strip to remove the metallic ions.

Final Inspection

The final step in the basic photomasking process is a visual inspection. It is essentially the same procedure as develop inspect, with the exception that the majority of the rejects are fatal. The one exception is contaminated wafers that may be recleaned and reinspected. Final inspection certifies the quality of the outgoing wafers and serves as a [illegible] of the develop inspection. Wafers that

Possible Process Cause	Contamination	Misalign	Undercut	Incomplete Etch	Wrong Mask	Pin Holes	C.D.'s	Visual Reject
Contaminated Etch	x		x	x				
Contaminated Stripper	x							
Contaminated H_2O	x							
Insufficient Rinse	x		x					
No Wet Agent				x				
Under Etch				x			x	
Over Etch			x				x	
Wrong Etch			x	x			x	
Hard Bake Too High			x	x			x	
Poor Develop				x			x	
P_2O_5 & SiO_2			x				x	
B_2O_3 & SiO_2				x			x	
Low Hard Bake			x					
Develop Inspect Escapes		x	x	x	x	x		

Figure 9.29 Final inspect rejects and process causes.

should have been identified and pulled from the batch at develop inspect are called *develop inspect escapes*.

The wafers receive a first surface inspection in incident white or ultraviolet light for stains and large particulate contamination. This inspection is followed by a microscopic inspection and a measurement of the critical dimensions for the particular mask level. Of primary interest is the quality of the etched pattern with underetching and undercutting being two parameters of concern. The table in Fig. 9.29 is a list of typical causes of wafer rejection found in the final inspection.

Mask Making

In Chap. 5, the steps of circuit design were detailed. In this section, the process used to construct a photomask or reticle is examined. The mask-making process is almost identical to the basic wafer-patterning operation (Fig. 9.30). In fact the goal is the same, the transfer of a pattern into the thin chrome layer on the glass mask surface. The two processes differ primarily in the exposure step. For mask making the image must be very precise or any image distortion will be translated to the wafer surface. For circuits with very demanding geometries, an

- Cut glass (or quartz) blank
- Clean glass
- Deposit chrome
- Inspect
- Clean
- Deposit resist
- Expose
- Etch
- Resist strip

Figure 9.30 Chrome mask process steps.

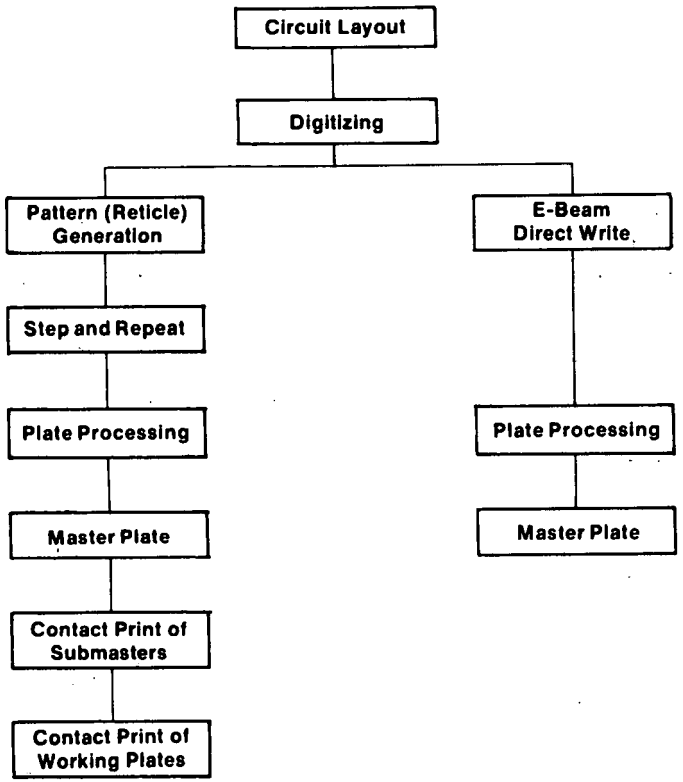

Figure 9.31 Mask-making flow diagrams.

electron beam exposure system is preferred, especially for the master plates (Fig. 9.31).

For most production plates and reticles, a pattern generator is used to establish the image in the photoresist. A pattern generator consists of a light source and a series of motor-driven shutters. The chrome-covered mask is moved under the light source as the shutters are moved and opened to allow precisely shaped patterns of light to shine onto the resist, exposing it.

After imaging by either electron beam or a pattern generator, the reticles or masks go through development, inspection, etch, strip, and inspection steps that transfer the pattern permanently into the chrome layer. Inspections are very critical since any undetected mistake or defect has the potential of creating thousands of scrap wafers. If the process calls for a lot of identical plates, called *working plates*, a special mask contact printer may be used to transfer the master plate pattern to a number of working plates.

With the advent of VLSI-level circuits a considerable amount of development had gone into the mask-making process. The masks and reticles must be virtually defect-free. There are now procedures to eliminate unwanted chrome spots and pattern pertusions with laser "zapping" techniques. There is also a technology to fill in missing pattern parts. Advanced circuit masks are made on low-expansion glass and quartz to minimize pattern distortions from temperature variations in the photolithography exposure and alignment steps.

Key Concepts and Terms

Develop inspect and rework
Dry etch methods
Dry stripping
Etch process
Final inspect
Hard bake methods
Hard bake process
Immersion develop
Mask making
Negative resist developers
Plasma descum
Positive resist developers
Puddle develop
Resist development
Resist stripping
Spray develop
Wet etch methods
Wet strip chemicals

Review Questions

1. Name the major methods of resist development.
2. What are the chemicals used to develop negative and positive resist?
3. What is the purpose of the hard bake step?